Ahnaf Zareef

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Technical Skills

Languages: C, C++, Verilog, Python, Bash
Protocols: I2C, SPI, UART, CAN, USB, Ethernet
Tools: Vivado, Vitis, Quartus, MicroBlaze, Altium, ESP-IDF, PSpice, MATLAB, TinyUSB
Platforms: Xilinx, ARM Cortex, ESP32, DE10-Lite, FreeRTOS

Experience

Firmware/ML Developer Intern Feb 2026 – Present
Carobot Learning & Research Organization *Toronto, ON*

- Developed an offline robotics development-kit to build and deploy ML models on an **ESP32-S3** for inference tasks on a block-based IDE.
- Implemented **C firmware**, implementing a composite device streaming live JPEG frames while receiving weights over serial, allowing for training and flashing over a single USB.
- Restructured IDE with **TensorFlow.js** implementing a **Neural Network** builder with configurable parameters for in-browser training for custom architecture.
- Wrote Conv2D, Dense, and Pooling forward-pass math in **Python**, generating **MicroPython** inference scripts.
- Evaluated variants, ruling out non-S/P boards for **PSRAM/OTG** limits, and benchmarked MobileNet V1 at **2.1x** device RAM before pivoting to raw image-trained models.

Power & Data Acquisition Member Sep. 2025 – Present
McMaster Solar Car Project *Hamilton, ON*

- Designed IV Curve Tracer PCB in **Altium** using a Darlington pair for high-gain current amplification, **ESP32** and a **Hall effect** sensor to characterize per-cell efficiency and detect faults.
- Developed protection circuitry: **MOSFET** switching on cell output, and **Zener** clamping on the ADC to prevent overvoltage damage.
- Wrote **C** firmware implementing an IV sweep with averaging, settling delays and offset calibration for more accurate readings.

Projects

I2C Master Controller

- Designed an **I2C** master in **Verilog** with a 4-phase bit timing scheme, separating each SCL and SDA.
- Implemented open-drain signaling and start/stop framing, releasing lines to pull-ups instead of driving high to prevent bus conflict.
- Verified the design with a testbench and slave model, deployed it as a memory-mapped device on **MicroBlaze** SoC with a C driver on the **Arty S7-25**.

XNOR-9

- Built a **Binarized Neural Network accelerator** on a **Tang Nano 9K FPGA**, replacing multiply-accumulate with XNOR-popcount, achieving **32**× model compression.
- Hit **95% accuracy** within the 8,640-LUT budget by redesigning the parallel datapath for sequential neuron compute after weight pruning and layer removal fell short.
- Built an **ESP32-S3** front-end capturing hand-drawn digits, streaming them to the FPGA over **UART**.
- Reshaped weight storage to match the FPGA's **BRAM** geometry, cutting memory **47%** to fit 270K weights.

Lidar Mapper

- Built **C** firmware for a spatial scanner, driving a half-stepped motor and VL53L1X ToF sensor over **I2C**, sampling 128 points per 360° sweep with per-step settling.
- Added interrupt-driven start/stop control and range validation, streaming polar data over **UART** to **MATLAB** for 3D point-cloud reconstruction.

Education

McMaster University Hamilton, ON
Bachelor of Computer Engineering, (GPA: 3.5/4.0) *Sep. 2024 – April 2028*